



- **Supports up to 16 LX8000 Packet Processing Engines:** Each LX8000 is a high-speed RISC CPU optimized for packet processing applications. A 16-processor system provides a performance of 7200 MIPS at 450 MHz and can process all seven networking protocol layers.
- **High-Speed Vortex Bus:** Moves up to 256 bits of data per cycle between the dual-port data memories of the CPUs and the customer's switch fabric or PHY interfaces achieving a bandwidth of 115 Gbits/s.
- **Block Transfer Controller:** Services block transfer requests for up to 64 threads. It can handle up to 16 simultaneously active transfers of configurable data path widths while maintaining packet ordering. (optional)
- **System Bus Bridge Architecture:** For a given application structures the system bus architecture to maximize bus frequency and preserve bus bandwidth.
- **The Test & Set Engine:** A Lexra Bus target that supplies up to 32 unique semaphores to control access to shared resources. (optional)
- **Ultimate scalability:** Equipment vendors can scale from a single LX8000 for a SOHO VPN to 16 LX8000 for an OC-192 router.
- **EJTAG Debug:** Extends the EJTAG 2.0.0 specification to the multi-processor and multi-context environment for on-chip debug. (optional)
- **Development Tools:** Available from third party suppliers supporting the MIPS architecture, including industry leaders Green Hills Software, Embedded Performance, and Wind River Systems.
- **Real-Time Operating System (RTOS) Support:** From industry leaders including NucleusPLUS™, ThreadX™, and VxWorks™.
- **Portability:** Available as a synthesizable RTL core or as a SmoothCore™, an optimized hard macro that has been ported to a specific foundry process. Foundry partners include IBM, TSMC, and UMC.

