



# LX4380 Product Brief

## High-Performance, Synthesizable RISC Processor

The LX4380 is a complete licensable, MIPS R3000-class RISC processor subsystem. It is optimized for high performance in a portable ASIC design methodology. The LX4380 achieves high-performance with a unique 7-stage instruction execution pipeline. Only positive-edge clocking is used throughout the design. Entire register-to-register clock cycles are allocated to cache access to increase performance and ease ASIC integration.

The LX4380 executes the 32-bit MIPS-I\* instruction set as well as Lexra extensions for improved embedded performance. The LX4380 incorporates selectable write-back, or write-through, cache controllers. Write-back was previously found only on 64-bit processors. The Block Move Controller (BMC) allows high-speed data or I/O transfer without interrupting the program.

Lexra's new MIPS R3000-style MMU (optional) comes with proven 3<sup>rd</sup>-party Linux support. Numerous additional customer configuration options ease ASIC integration. The LX4380 is supported worldwide by leading development tool vendors.

### TARGET APPLICATIONS

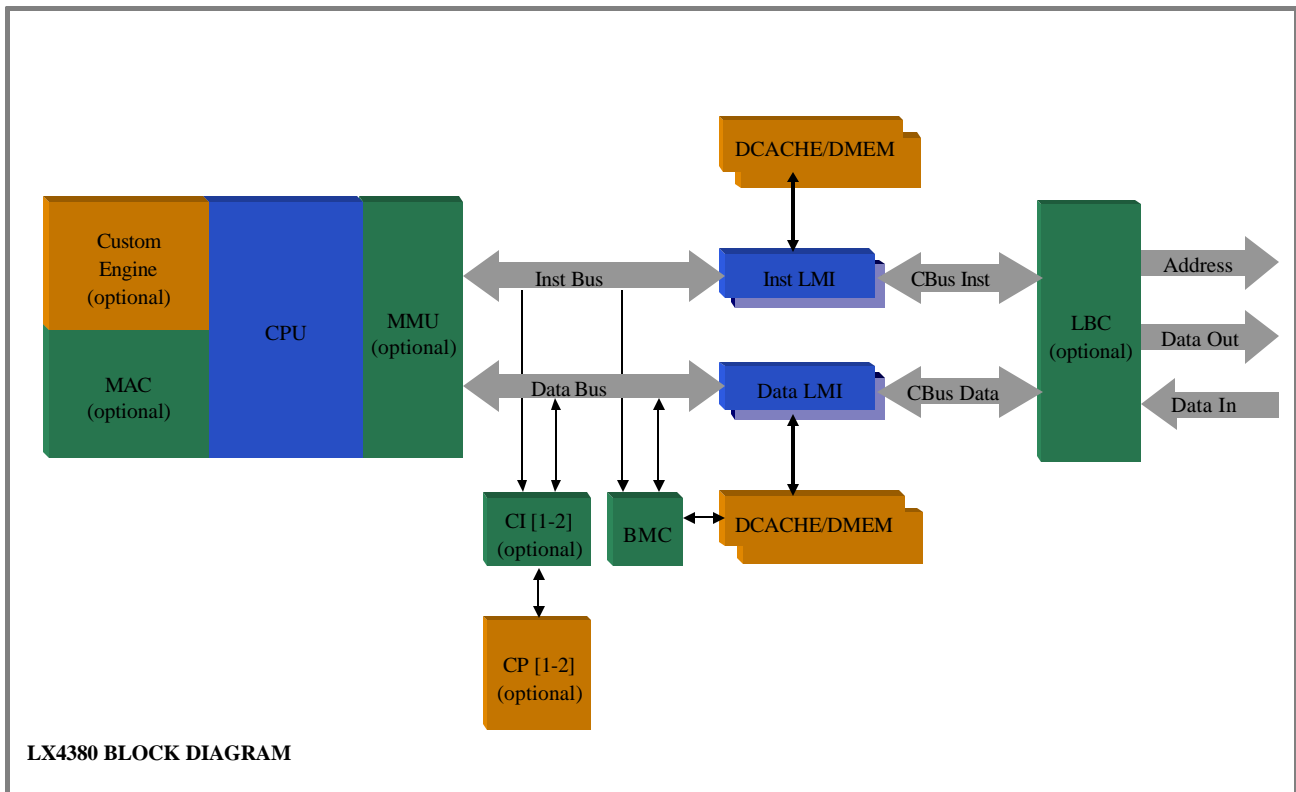
- Consumer electronics appliances
- DSL controllers
- Interactive digital TV devices
- Multi-protocol web servers
- Office automation

### SPECIFICATIONS

RTL Model synthesized in a typical 0.15µm ASIC process:

- 300 MHz worst-case operating conditions
- XX MHz typical operating conditions
- 1.0 mm<sup>2</sup> (base configuration)
- Power dissipation: 44 mW (base configuration)
- Operating temperature: 125° C junction
- 1.2V core

Also available as a hard macro (SmoothCore™).



## FEATURES – REQUIRED BLOCKS

- **High-Performance, Synthesizable CPU**
  - 7-Stage instruction execution pipeline
  - MIPS-I ISA
  - Lexra CPU extension:
    - Single-cycle 64-bit Load
    - Eight (8) prioritized, vectored interrupts
    - Conditional moves
    - Block Move Controller (BMC) – high-speed background DMA of data, I/O.
- **Local Memory Interface (LMI)**
  - 0 - 64 KByte ICache, 0 - 64 KByte Dcache
  - Direct-mapped or 2-set associative
  - Configurable line size (16-128 Byte)
  - Selectable write-through or write-back
  - Physically-indexed, physically-tagged
  - 0 – 256 KByte fixed IMEM, DMEM

## FEATURES – OPTIONAL BLOCKS

- **Lexra Bus Controller (LBC)**
  - Separate unidirectional addr, data in, data out
  - 0 – 64 Byte write buffer
  - Variable size burst mode
  - Several clocking alternatives
- **Memory Management Unit**
  - MIPS R3000-style
  - Proven 3<sup>rd</sup>-party Linux support
  - 2-entry ITLB, DTLB; 16/32/64-entry JTLB
  - 4 KByte page size
- **MAC Unit**
  - Single-cycle 16x16b mult, mult-add, mult-sub
  - Two-cycle 32x32b mult, mult-add, mult-sub
- **Extended JTAG (EJTAG) 2.0.0 Debug**
  - Single-stepping
  - Instruction and data address breakpoints
  - Real-time PC trace
- **Custom Engine.** Customer can add application-specific ALU ops. 3-register operand or 2-register/immediate formats are available.
- **Coprocessors.** 1-2 Customer-designed Coprocessors can easily be attached to Lexra-supplied Coprocessor Interfaces (CI).

## DEVELOPMENT TOOLS

The LX4380 is supported by the most popular development tools in the industry.

- Green Hills MULTI 2000 IDE.
- Embedded Performance, Inc. MAJIC emulator probes provide a high-speed hardware interface to the LX4380 using Extended JTAG on-chip debug interface and powerful industry standard debuggers.
- Lexra Instruction Set Simulator (ISS). Cycle-accurate model of the LX4380 to enable system-level software development and performance analysis.
- Lexra Hardware/Software Development Board. Enables PLD prototyping of systems incorporating the LX4380. The development board also facilitates early software development and debug.
- Available Operating Systems. Linux (Amirix Systems), NucleusPLUS (Accelerated Technology, Inc.), ThreadX (Express Logic), VxWorks (Wind River).
- Lexra GNU Tools. Standard GNU tools with Lexra extensions.

## CONTACT INFORMATION

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