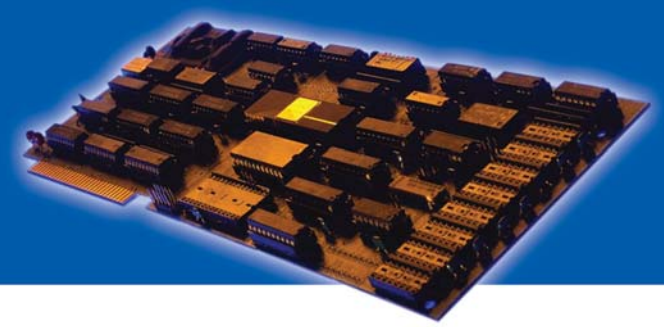
LEXRA

SP-1 STREAM PROCESSOR
ADVANCE PRODUCT BRIEF



HIGH-TOUCH NETWORKING

MULTI-PROCESSOR IC FOR DEEP PACKET PROCESSING

Lexra's Stream Processor (SP-1) IC provides the ultimate in both the performance and flexibility required to execute demanding "high-touch" network communication applications on multiple 1 Gbps packet streams. The SP-1 includes four (4) LX4580 MIPS32™ RISC CPU's that operate in parallel on independent instructions for optimized packet processing. The CPU's incorporate Lexra's innovative *fine-grained Hardware Multi-Threading (HMT)* technology, resulting in high CPU performance even during the servicing of cache misses.

The CPUs are interconnected with shared resources through a high-bandwidth full-duplex Crossbar, which can sustain over 300 Gbps peak bandwidth. Connected to the Crossbar is the Memory Subsystem, which includes an L2 cache, a cache coherency engine, and two 64-bit interfaces to external DDR SDRAM, resulting in a total SDRAM bandwidth exceeding 50 Gbps.

Typically, packets enter and exit the SP-1 through the three (3) full-duplex Gigabit Ethernet interfaces. Connection to a control processor or specialized co-processor is accomplished via the 32-bit PCI-X interface. The Ethernet and PCI-X interfaces include intelligent DMA Controllers that allow packets to be queued in SDRAM without CPU intervention and with minimal use of interrupts. Packet mapping engines resident inside the DMA Controllers direct incoming packets to individual queues.

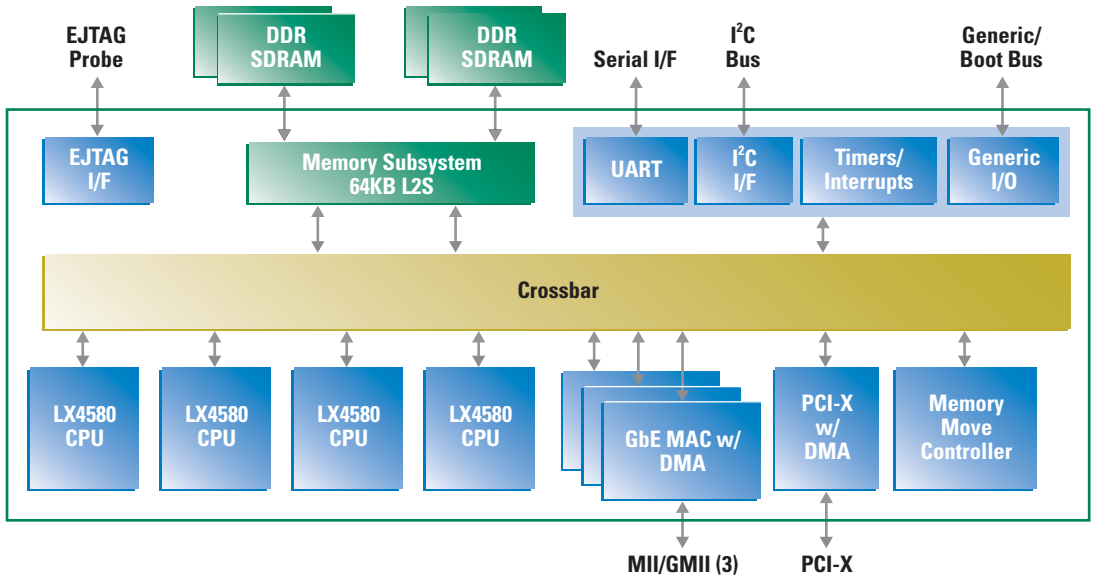
To permit easy integration into a wide variety of systems, the SP-1 incorporates several industry standard I/O interfaces, including a generic boot bus and an I²C interface for simple, low-cost connections to boot EPROMs and microcontrol components. Also included are interfaces for both serial communications and embedded debug (EJTAG).

TARGET APPLICATIONS

Enterprise Edge Application Servers
VPN, Firewall, and Intrusion Detection
Edge Access Routers
Network Attached Storage and Storage Area Network Servers

SPECIFICATIONS

- Technology: 0.13 µm CMOS
- 500 MHz Processor Clock
- 2800 Dhrystone 2.1 MIPS at 1.4 DMIPS/MHz/CPU
- Power Dissipation: 5 W (worst-case)
- Voltage: 1.2 V
- Operating Temperature: Commercial (0ºC to 70ºC)
- Package: 676-pin PBGA



HIGH-TOUCH NETWORKING

FEATURES

(4) LX4580 RISC CPUs

- 500 MHz Processor Clock
- MIPS32™ Release 2.0 ISA
- Lexra CPU extensions:
  - Hash with key size 4 to 24 bits
  - Dual 16-bit ones-complement add
- Fine-grained Hardware Multi-Threading (HMT)
  - Four threads of execution per CPU
  - Unique register set and TLB per thread
  - Execution alternates among threads
  - Hides latency due to cache misses
  - Up to 3X performance benefit compared to single-threaded CPU
- 7-stage execution pipeline
- Independent instruction and data caches per CPU
  - 64 KB L1 instruction cache
  - 16 KB L1 data cache
  - 4-way set associative, parity protected

High Bandwidth Crossbar Interconnect

- Connects CPUs, DMA Controllers, Memory Subsystem, and I/O Interfaces
- Incorporates distributed queuing to eliminate head-of-line blocking
- Runs at one-half CPU frequency (250 MHz)
- Over 300 Gbps internal bandwidth

High Performance Memory Subsystem

- On-chip L2 cache
  - 64 KB, shared by all CPUs
  - 4-way set associative, parity protected
  - Optimized for shared data
- (2) 64-bit DDR SDRAM interfaces
  - Interfaces to 133 MHz and 200 MHz DDR SDRAM
  - ECC protected memory
  - 32 MB to 8 GB external SDRAM
  - Over 50 Gbps SDRAM bandwidth
- Coherency engine
  - Hardware enforced coherency between main memory and all caches
  - 64 byte cache line size
  - Manages CPUs' L1 caches via MESI protocol

(5) DMA Controllers

- Supports background transfers between I/O interfaces and SDRAM, or between two SDRAM locations
- Memory resident queues and buffer descriptors
- Minimal use of interrupts, minimal CPU overhead
- Three DMA Controllers dedicated to Ethernet Interfaces
  - Sustainable 64 byte packet transfers
  - Programmable hashing of packet header fields to determine input queue assignment
  - Software controlled queue assignment among threads
- One DMA Controller dedicated to PCI-X
- One Memory-to-Memory DMA Controller

Industry Standard Interfaces

- (3) Gigabit (10/100/1000) Ethernet Interfaces
- (1) 32-bit, 133 MHz PCI-X Interface
- (1) 32-bit Generic/Boot Bus
- I²C Interface
- RS232 Serial Interface with UART
- EJTAG Interface

DEVELOPMENT TOOLS

Support for Leading Operating Systems

- Linux® SMP, VxWorks®

Extensive On-Chip Debug Features

- EJTAG
- UART with RS232 Serial Interface

Complete SP-1 Development Platform

- C/C++ development tool chain
- Development board
- Device drivers and abstraction layer
- Sample code

CONTACT INFORMATION

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