Whitepaper

7-Stages
Lexra's New High-Performance ASIC Processor Pipeline

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Introduction

The architectural problems faced in developing a high-performance pipeline for a licensable processor include most of the same challenges of traditional processor architecture, but a number of additional difficult challenges as well. As in any pipeline design, the tasks should be well-balanced among the different stages. However, licensable processors are often integrated into ASICs using a conventional ASIC design flow. The processor must be synthesized then placed-and-routed using conventional ASIC design tools. It is desirable that the performance of the processor architecture be relatively insensitive to the quality of the floorplan and place-and-route. The problem is compounded by the configuration options typically offered by licensable processors. The most important among these configuration options - variable size Icache and Dcache - can cause wide variations in the results actually achieved by ASIC designers. Worse, the results are hard to predict. These problems can be mitigated somewhat by careful attention to the backend design or by the application of hard, rather than synthesizable, processor cores. However, these strategies undermine two key advantages: technology portability and ease-of-use that the customer often wants to achieve by licensing processor IP. This Whitepaper will describe Lexra's new 7-stage processor pipeline and its advantages of both speed and suitability for synthesizable ASIC design.

Requirements

The two key principles in developing Lexra's 7-stage pipeline (Figure 1) were:

1. Only the positive-edge of the system clock should be used throughout the design,
2. Critical paths between major subsystems should be avoided.

When MIPS Technologies, Inc. (MTI) introduced licensable versions of its RISC processors, it also reworked its traditional 5-stage pipeline to minimize but not eliminate dependence on the falling edge of the clock. The MIPS32 4K™ pipeline is illustrated in Figure 2. The reader will observe that the negative clock edge is used in each pipeline stage; for instance the ALU operations are initiated on the

falling edge, while the register file read, which feeds the ALU, is initiated on the previous positive edge. The problem, familiar to full-custom processor designers as well, is that clock duty cycle is far harder to control than clock period. This problem is exacerbated in deep sub-micron ASIC technology where clock duty cycles are subject to +/- 10% worst-case variation. As a result the actual access time allocated to the 4K register file read will vary widely with technology and place-and-route results.

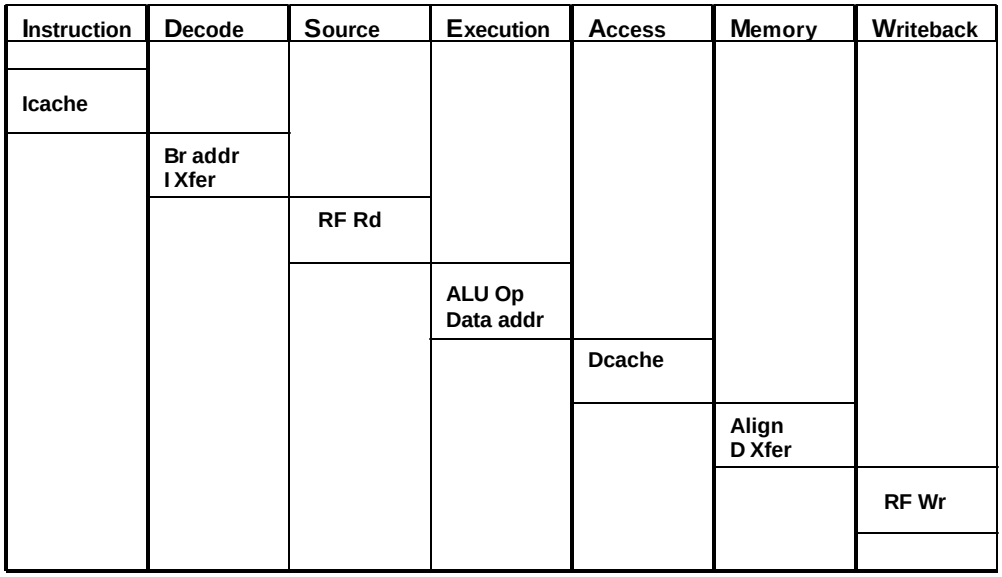
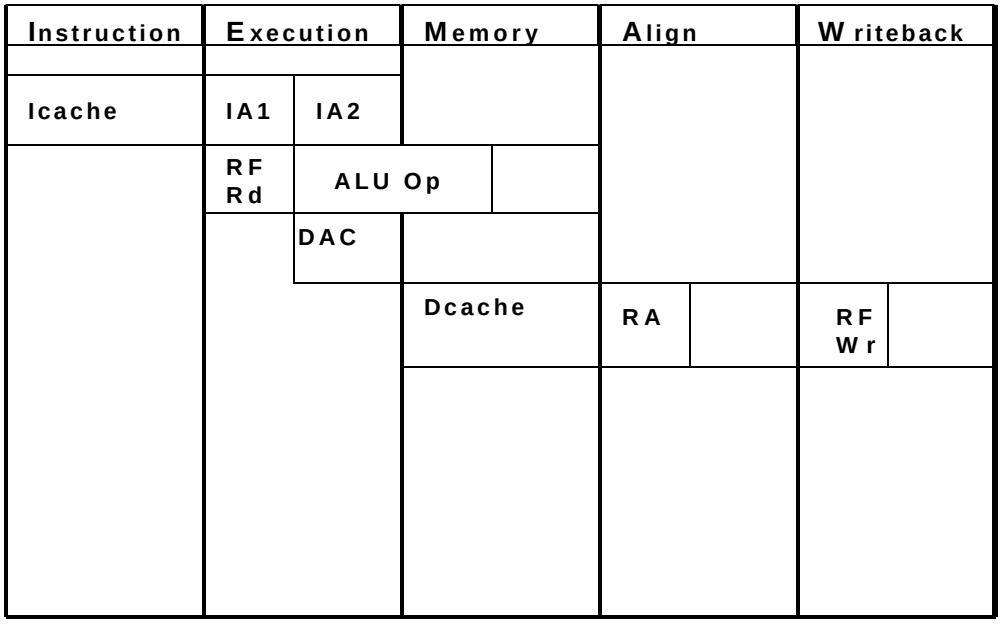


Figure 1: Lexra's 7-Stage Pipeline



Source: Embedded Processor Forum, May 1999.

Figure 2: MTI's MIPS32 4K™ 5-Stage Pipeline

The most important inter-block critical paths in a processor often include the address and data buses, for Icache and/or Dcache. If the memory access is part of the inter-block critical path, performance becomes very sensitive to layout results. A starting point for the architecture of Lexra's 7-stage pipeline was the allocation of a full address-register-to-data register clock cycle for RAM access. Figure 3 is a simplified illustration of a 2-set associative cache read access path in Lexra's earlier 5-stage RISC pipeline. Figure 4 illustrates the same path in the new 7-stage pipeline. The 7-stage pipeline provides the maximum cache clock speed for caches. This is critical because ASIC designers have little, if any, control, over their memory designs. More subtly, the timing convergence for a particular clock frequency and cache size will be more predictable, less subject to degradation caused by parasitics introduced by the memory placement itself.

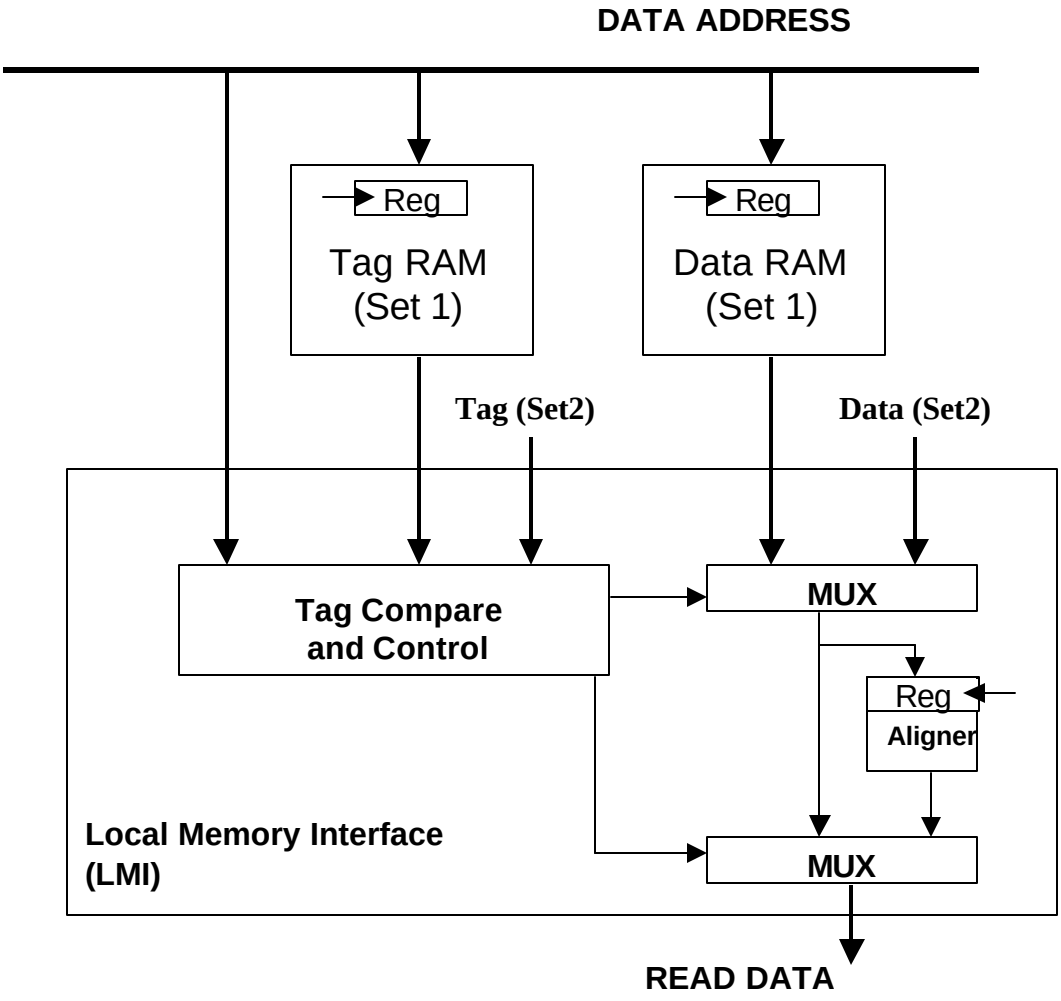


Figure 3: Lexra's Dcache Read Path – 5-Stage Pipeline

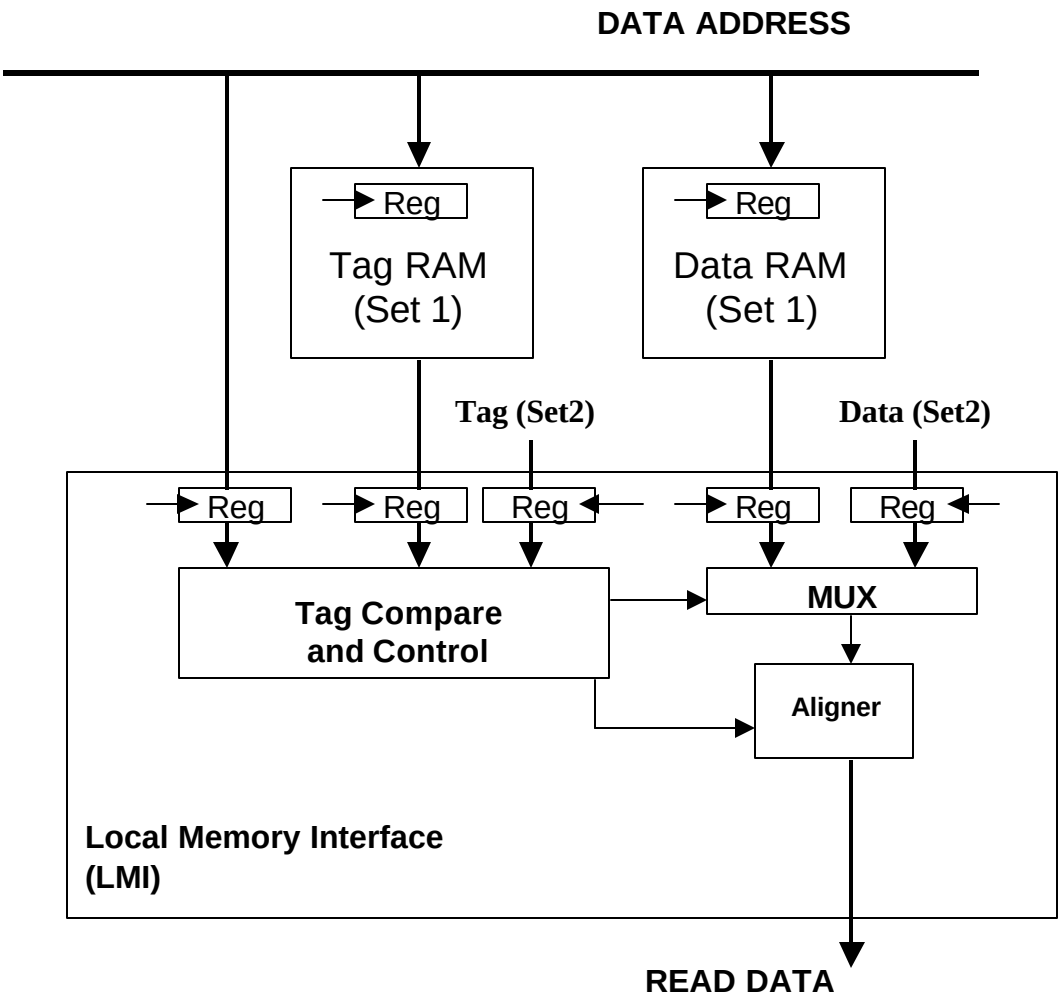


Figure 4: Lexra's Dcache Read Path – 7-Stage Pipeline

The New 7-Stage Pipeline

Lexra's 7-stage pipeline is illustrated in Figure 1. Icache access takes place in the Instruction stage, similarly the Dcache access takes place in the Access stage. We emphasize, a full system clock cycle is devoted to the RAM access. Address, instruction and data bus transfers to and from the RAMs take place in other pipeline stages which are far less critical because they do not include the memory access. The Decode stage includes Icache tag verification, set selection and Instruction transfer. Similarly, the Memory stage includes Dcache tag verification, set selection and read data transfer. For data memory transfer, the Memory stage also includes partial word alignment shift. (Lexra's earlier 5-stage pipeline required a stall cycle for partial word alignment.)

Similarly, register file read access along with forwarding logic is allocated the full Source stage of the pipeline. The forwarding paths are 32-bit buses from the ALU output, the ALU result register, the Memory stage, and the Writeback

stage to the two ALU input registers. The forwarding paths are not only routing intensive, but in the case of the forwarding path from the ALU output, they are also time critical. The 7-stage pipeline gives the ASIC place-and-route the best possible chance to succeed. By contrast, the MIPS32™ 4K™ pipeline allocates only a half-cycle to the register file read and forwarding paths.[1]

Performance Results

The new 7-stage pipeline will be deployed across Lexra's entire product line of RISC, DSP and network communications processors, beginning with the third-generation LX4380 RISC processor. The table below summarizes performance results for the LX4380.

	LX4380
Technology	TSMC 0.15 µm
Library	Artisan
Icache	16 KB direct-mapped
Dcache	16 KB direct-mapped
Synthesis	Synopsys Design Compiler V99.10
Place-and-route	Avant! Apollo V200.2
System clock	**300 MHz**

These results were obtained on the post-layout database for worst-case conditions of process, voltage and commercial temperature. Similar results can readily be achieved by customers without special understanding of the processor's micro-architecture. In fact, Lexra has achieved over 300 MHz worst-case in a number of 0.15 µm ASIC technologies for memory sizes up to 64 KB.

Comparing an idealized 7-stage pipeline to an idealized 5-stage pipeline, the system clock speed of the 7-stage pipeline will be higher in proportion to the number of pipeline stages; that is, the 7-stage pipeline clock will be 7/5 = 1.4 times faster. Some of this performance is sacrificed by additional stall cycles which occur in the 7-stage pipeline upon: a) branch prediction failure (as a consequence of allotting a full register-to-register cycle to Icache) and b) occasional load interlock stalls (as a consequence of allotting a full register-to-register cycle to Dcache.). Our frequency analysis of these events in application programs results in a net performance gain of about 30% in the idealized 7-stage pipeline, as compared to the idealized 5-stage pipeline.

In fact, no real-world pipeline meets the ideal uniform-loading standard. As we have seen, the MIPS32™ 4K™ pipeline allocates less than half the time to register file read and forwarding as the Lexra 7-stage pipeline. In some

[1] The 4Kc register file is "write-though"; that is, in the case that the same register is updated and read in a particular cycle, the new data must be passed through the register file from the write port to the read port. This write-though path slows the register file performance, further burdening the already overburdened layout.

configurations, this may translate into a performance advantage of 2X for Lexra using equivalent technology and backend resources.

As another comparison point, consider the ARM9 5-stage.[2] The Execution stage of the ARM9 includes a requirement for barrel shift followed by an addition or subtraction. In Lexra's Execution stage either of these operations – shift or subtract – is allocated the full stage. Squeezing these two operations into one cycle, can degrade ARM's system clock by up to 50%, compared to Lexra, in comparable implementation technologies.

Figure 5 illustrates the performance of Lexra's LX4380 as a function of Dcache size. In all three Figure 5 graphs, Icache size is fixed at 16 KB. For Dcache sizes smaller than 64KB, the rate-limiting paths are flop-to-flop within other major modules. Furthermore, the graph shows the insensitivity of the ASIC timing convergence to the large range of memory sizes on the floorplan and inter-block buses. For comparison, the LX4189 uses a 6-stage pipeline quite similar to Figure 1, except that the Access stage is missing. Not only is the performance less that for the LX4380, but the graph of LX4189 speed vs. performance is quite sensitive to Dcache size. As a result, timing convergence for specific Dcache sizes, in differing technologies is more difficult than for the LX4380. The speed graph for Lexra's earlier LX4180 is also illustrated. The LX4180 uses a 5-stage pipeline similar to Figure 1, except that both Decode and Access stages are missing. In other words, for both Icache and Dcache, the access paths, tag validation, muxing, and bus transfers are included in the same critical path. The flat graph up to 64 KB Dcache, simply indicates that the 16 KB Icache access or other flop-to-flop paths, are tougher critical paths than the Dcache path in the LX4180. For this reason, Lexra first added the 6th stage, the Decode stage, to create the LX4189[3]. With the new generation LX4380, the pipeline has arrived at 7-stages, its ultimate destination, where Icache and Dcache are both treated optimally.

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[2] Microprocessor Report, December 8, 1997. The earlier ARM7 used a 3-stage pipeline, ostensibly to save area and power. This approach was later followed by one MIPS licensee (LSI Logic) in some of its implementations. With deep submicron technology, the argument for 3-stage pipelines, has long since lapsed as the newer ARM9 testifies. The area and power savings of the 3-stage pipeline is real but very slight in comparison with the performance degradation.

[3] Another reason for the priority our development plans assigned to the Decode stage over the Access stage is that customer's typically have needed larger Icache than Dcache.

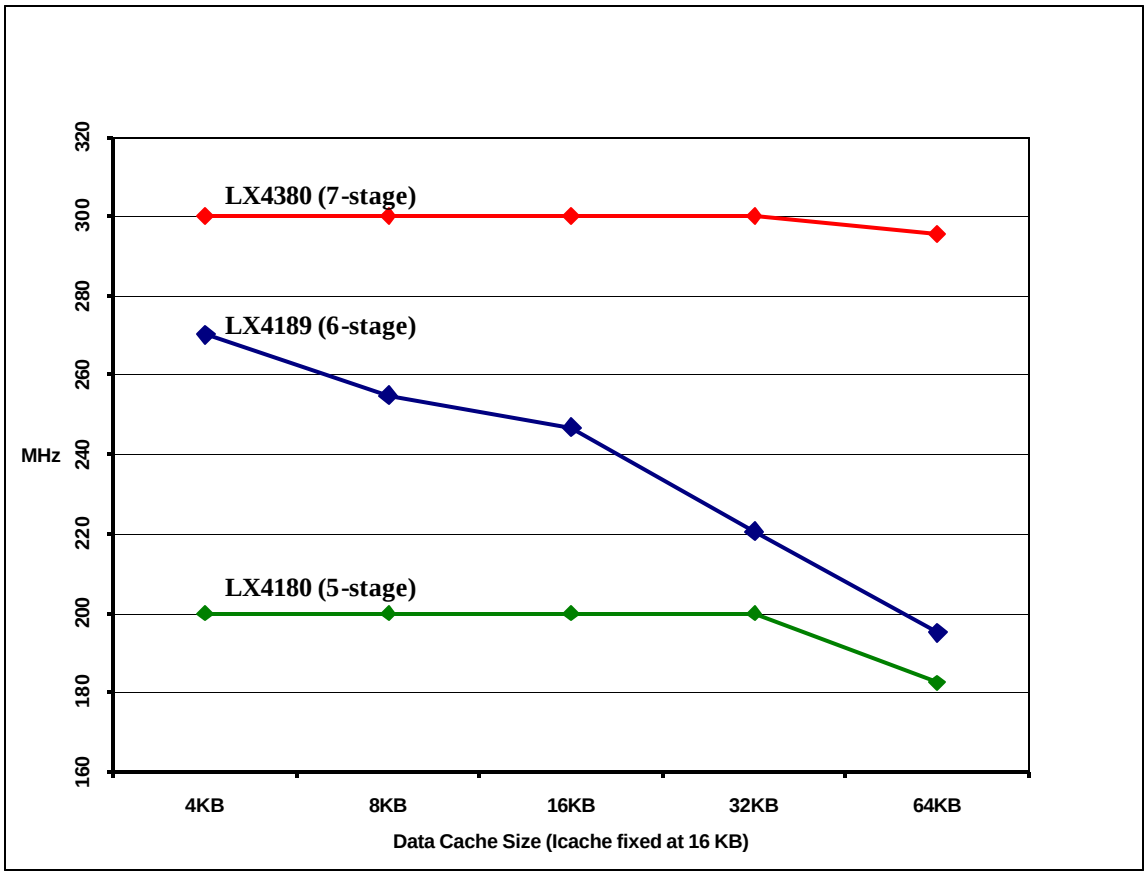

Figure 5: System Clock Frequency vs. Dcache Size

Conclusion

This Whitepaper has described how Lexra's new 7-stage pipeline overcomes the challenge of achieving a high-performance processor pipeline in a portable, easy-to-implement ASIC technology. Only positive edge clocking is used throughout, and additional pipeline stages minimize the dependence of critical paths – notably cache access – on place-and-route. We expect that future scaling of memory speeds, switching speeds and parasitics will increase the performance advantage of Lexra's 7-stage pipeline.