Surprise: IP Integration Problems Eliminated Through Streamlined Interconnect

A smartphone has almost all of the features of a PC and many many more such as GPS, accelerometers, and NFC. New product requirements for ever higher levels of integration are causing SoCs to become more complex. This challenges performance, cost, power efficiency, reliability, and time-to-market. Since the number of functions is increasing while total die size is not, SoCs are increasingly constrained by the growing number of wires required to make connections to the different IP blocks within the design.

The increase in net count and total wire length to route plagues design teams with routing congestion. The drawbacks are so significant that they often negate the performance, cost, power efficiency, reliability, and time-to-market advantages of chosen IPs. This can cost chip companies opportunities for critical design wins in high-volume or emerging-growth markets.

The place and route (P&R) stage of chip design is critical for abating wire congestion. Designers must design for constraints on:

- Die size
- Power consumption
- Latency
- Metal mask layers
- Defect rate
- Wire lengths
- Mask costs
- Critical paths
- MTBF reliability
- Schedule

The interconnect fabric is the IP with the most significant effect on all of the constraints. Even the best internal interconnect fabric IPs do not address all of these constraints optimally. Each generation of process technology and each member of a chip product line bring new considerations to the forefront. These considerations, affected by routing congestion, are exacerbated with each generation since wire widths do not shrink as fast as transistors. As a result, the silicon area lost to wire routing congestion is increasing. This trend contributes to larger, more spread-out floor plans that decrease the amount of dies each wafer can yield and increase the amount of defects per die. A more spread-out floor plan also makes wire routes longer, which reduces the predictability of critical paths.

One way to decrease floor-plan size is to add more metal layers to the fab process. However, an increase in layers and masks adds to manufacturing expense and also increases defect rates.

A packet-based network-on-chip (NoC) interconnect fabric alleviates routing congestion. The top semiconductor design teams, who are building the most highly integrated chips, are addressing congestion by adopting NoCs for the interconnect. This is because packetizing allows information to be sent sequentially with configurable degrees of serialization. This allows the throughput requirements of links within the chip to be met with a minimum amount of wire metal.

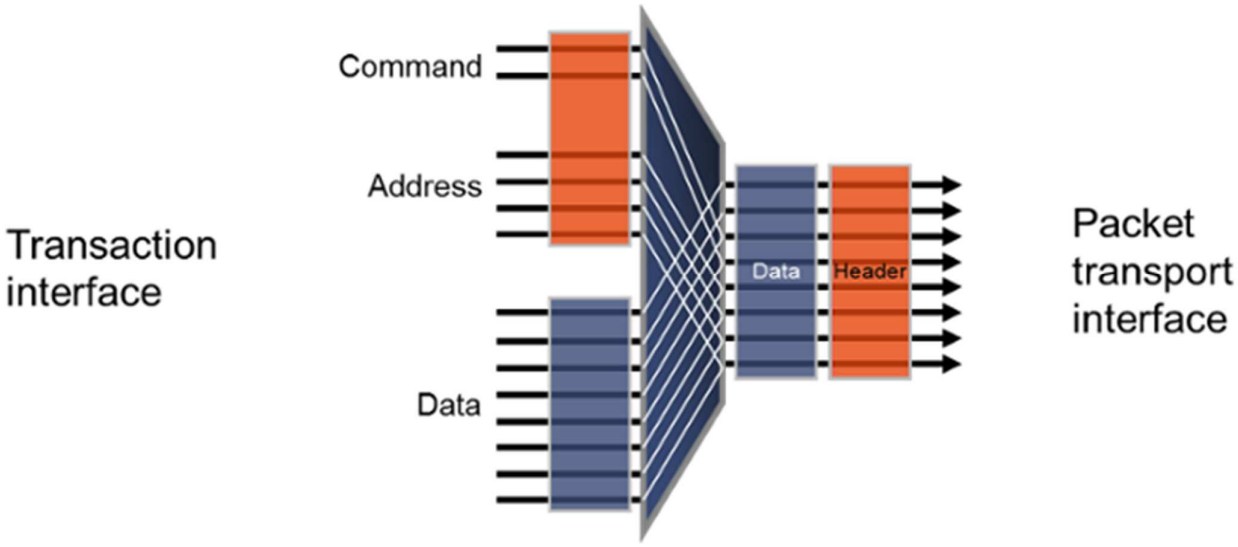

Figure 1: Packetization places the address and control signals on the same wires as the data.

Packetization and serialization reduce the size and maximize the temporal utilization of the buses connecting IPs.

- Packetization takes the SoC transaction data and places them on the same wires as address, control and command signals. This results in fewer wires to move data around on the chip compared with using standard socket or transaction interfaces.
- With serialization, the data can be transmitted on even narrower channels, thus shrinking wire count on chips. Designers can also trade wires for throughput and transaction latency to gain a greater degree of freedom compared to standard interconnect designs.

Serialization and packetization can cut in half the total wire length of the top-level interconnect fabric to route within a chip.

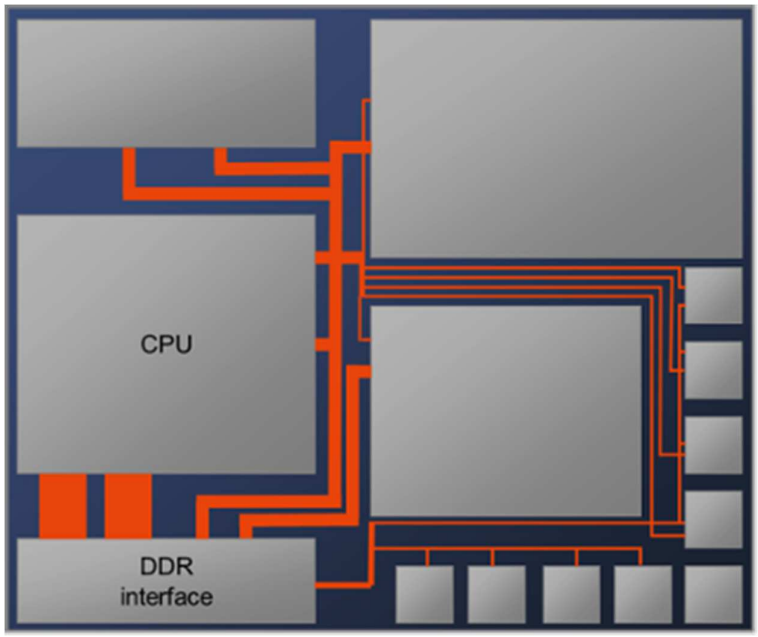

Figure 2: Packetization and serialization reduce the total wire length of the top level interconnect by 50%.

A minimal configuration of a 64-bit AXI interface requires 272 wires. A 64-bit packet-based channel within an Arteris NoC delivers nearly the same bandwidth with just 157 wires. Furthermore, the channels within an Arteris NoC can adapt serialization, with no additional latency, to provide more or less bandwidth as required by each link.

The bottom line is that a NoC requires far fewer wires to move data between IP blocks than older interconnect technologies like buses and crossbars. This provides physical design benefits that equate to better quality of results and faster design closure at the back end of the design process. NoC technology is a front-end solution to a back-end problem.

A NoC provides:

- Accelerated time to market
- Smaller die size
- Optimized floor plan
- Lower cost
- Higher performance
- 50 percent reduction in total wire length
- Reduced power consumption

Arteris is the inventor and leading provider of NoC IP. Arteris FlexNoC reduces complexity for SoC designs and enables faster time to market. Design teams are achieving better results in terms of meeting product requirements. This enables them to create the industry's most competitive products.

Arteris goes into greater depth about the advantages of a packet-based NoC approach and provides more detail on the benefits of serialization in a white paper entitled Routing Congestion: The Growing Cost of Wires.

Jonah Probell is a Senior Solutions Architect at Arteris.