TEN REASONS INTERCONNECT MATTERS

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Interconnect is the Rodney Dangerfield of IP blocks. It gets no respect. It connects hundreds of disparate IP blocks, each with hundreds of interface signals, and dozens of transaction protocol attributes. It does it in a way that each IP need not know the protocol details of any other. It also provides for the data access requirements of each IP, and does it physically distributed across the chip floorplan. Interconnect fabric technology is sophisticated, and very important for modern chip designs. Following are ten reasons why interconnect matters.

1. CRITICAL TO CPU AND GPU PERFORMANCE IN SOCS

The interconnect fabric is the connection between processors and coherence controllers, last-level system caches, and DRAM memories. Increases in CPU or GPU performance are only useful with a corresponding increase in interconnect bandwidth. There are many detailed considerations required for a low-latency interconnect in a high-performance CPU-based SoC.

2. LAST IP TO CONFIGURE IN A CHIP DESIGN

The impact of schedule delay increases as a project approaches its conclusion, and the last step is the most significant in avoiding delay. Even though interconnect is a front-end RTL IP, it is the last one to be configured since it depends on the configuration of all others. A thoughtfully designed interconnect fabric avoids costly timing closure problems and design rule violations that cause delays in the routing and post-route optimization stages of chip designs.

3. LONGEST PHYSICAL CONNECTIONS BETWEEN CELLS

The interconnect fabric connects and arbitrates between all of the IPs on a chip, even ones that are physically far apart. As a result, interconnect logic signals fan out over very long distances, requiring many buffers, inverters, and metal layers. For many links in the interconnect fabric, wire length capacitance delay is much larger than gate switching delay. This makes it necessary to carefully pipeline the logic and constrain the placement of pipeline stage flops within the floorplan.

4. Big impact on wire routing congestion

Because the interconnect fabric has long wires, and aggregates wide, high bandwidth buses to centralized locations, the interconnect tends to have areas of high place and route congestion. Packetization, serialization, and careful design of a NoC-based interconnect network topology minimizes congestion within the bandwidth requirements of a chip design.

5. Contains the power-disconnect logic of the SoC.

Powering down processing units and interfaces that are not needed in different use cases is critical to conserving energy in batteries and also managing overall power consumption and heat. The easiest and safest way to do so is in a NoC interconnect, which provides a single universal disconnect protocol to a system-level power manager and also ensures the correct completion of pending transactions before power-down.

6. Provides the bandwidth and meets latency requirements

Different IPs have different quality-of-service (QoS) requirements. CPUs, cameras, and displays are latency critical. DMA engines and video codecs are bandwidth hungry. UARTs are neither. The interconnect handles IPs of different frequencies, sizes, and protocols and serves as the place to implement QoS controls to avoid performance degradation in unexpected use cases in the field.

7. Resilient to soft errors and defects

Interconnect IP has particularly high wire to gate ratio. That makes it more susceptible than many other IPs to manufacturing defects, soft errors, and wear-out failures. Modern NoC interconnect fabrics offer configurable levels of redundancy to provide error resilience for automotive, industrial, and enterprise-critical storage applications.

8. Carries all of the most secure traffic

The safest way to thwart hackers is to make it physically impossible to access sensitive interface, storage, and cryptographic IPs in chips. The interconnect is the physical connection between all of them. Hardware firewalls in the interconnect fabric are, by far, the safest way to protect sensitive information passing through SoCs.

9. Opens debug visibility into all other IPs

CPUs have debug ports that software developers can use to bring up their software. That is not the case for the other 99% of IPs in the chip. Because the interconnect sees the reads and writes of all IPs in the chip, NoC-based interconnect debug probes give an otherwise impossible level of traffic visibility. That is valuable for software development, but is also used by some clever programmers for real-time optimization in the field.

10. The complexity and value of advanced interconnect is unappreciated

To the uninitiated, an interconnect fabric is a bunch of wires. The interconnect in modern chips is comprised of millions of gates of standard cells. The logic is used for buffering, clock domain crossing, muxing, and scheduling. The NoC-based interconnect fabric IP offerings on the market today are sophisticated pieces of IP that have been built with the work of hundreds of engineer-years. They are highly optimized for total system power reduction and ease of integration. The wise project leader will take advantage of third-party NoC interconnect IP, such as that offered by Arteris.

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