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BY SAM ROSEN

Combining Low Power with High Performance

Key to Successful Embedded Processors

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The ARM processor has been perceived for too long as the only embedded processor offering the best power consumption. When it first appeared more than a decade ago, this was certainly the case, but rapid advances in process technology and architectural enhancements in other processors have undermined that advantage. Furthermore, the power advantage has actually accrued to new designs that have leveraged advances in process technology.

This article will describe what features of the ARM instruction set gave it its initial power lead. It will then describe how Lexra's 5180 has advanced to surpass ARM's strength. Thus, an application such as a digital camera, powered by Lexra, could achieve longer battery life with the same feature set or could add additional features such as a powerful web browser while maintaining the same battery life.

Process Technology in Power Consumption

When ARM introduced its embedded processors in the early 1990s, semiconductor process technology with 0.5 micron feature size was just beginning to become available. The predominate voltage-powering chips produced was 5.0 volts. The CPU core on a typical ASIC design could easily represent half the die area and could consume as much as half the chip's power. Power-hungry I/O drivers and a customer's own logic gates accounted for the rest of the power draw.

As process technology shrank to 0.35 and 0.25 micron feature sizes, voltage dropped to 3.3 v, while the number of gates possible in a given die area began to soar. Today, as process technology advances, feature sizes of 0.15 and smaller are becoming available. Voltage levels have dropped from 3.3 volts to below 2.5 volts. At these smaller process geometries, the CPU core in an ASIC design made up increasingly less of the total ASIC design gate count.

A power savings of 15 percent in an IP core representing 50 percent of an ASIC is far more meaningful than the same power savings in a IP core representing 10 percent or less of a larger system-on-a-chip (SoC) design. In these systems, increasing the functionality of the core is just as important as decreasing the power consumption. In addition, I/O pins dissipate a large percentage of the power in a system. Today, most of these designs are becoming pad-limited, with pin counts in excess of 200 pins. As a result, I/O began to represent the power hog on most new chips. System on a chip design with a powerful microprocessor allows reduction in the number of pins in a system without reducing the functionality of the part.

Full-Custom vs. RTL

When ARM licensed its IP core, it chose to implement its processors using a full-custom, hard-core approach. By contrast, Lexra chose to offer a soft-core RTL design and a hard-core one. The type of cores available, hard or soft, has an impact on designers using different IP. A system company that creates its own SoC design using third party IP might prefer a soft-core design, while an fabless IC company that builds application specific standard products (ASSPs) might prefer a hard-core design.

Until recently, ARM only supplied a hard core ported to a particular IC manufacturer such as Samsung, LSI Logic, and Texas Instruments. By manually optimizing the processor's device sizing, clock tree, and power lines during porting, the full-custom approach can reduce power consumption. The tradeoff is that you cannot rely on a standard tool flow, and the final design is targeted to a single foundry.

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System company chip designers allotted a certain area in their larger chip's floorplan to represent an ARM core. They designed the rest of their circuit around the block and then had an IC vendor stitch the two parts together during manufacturing. Fabless IC companies that wanted an ARM core were forced to use an IC vendor that offered the core in its library.

In contrast, Lexra implements its processors in RTL, which allows a standard synthesis-based design flow. This approach is faster, which means designers can go to market sooner, and target a final design to any foundry, which is ideal for fabless IC companies. Because some fabrication technologies offer better power characteristics than others,

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they can weigh power issues against time-to-market and cost considerations. To achieve higher performance, Lexra can port IP to a target foundry.

An advantage to using an embedded processor that comes in RTL form is that designers can make implementation choices that best suit design goals. If designers want to minimize power, for example, they can optimize cell sizes to take advantage of a library's low-drive cells. Designers can optimize the processor's clock and buffer trees for power as well. They also can specify alternative logic that is slower (and sometimes larger) but dissipates less power. If designers intend to run the LX5180 at speeds less than 66 MHz, they also can reduce power consumption by implementing a processor using lower-voltage logic.

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ARM's Initial Power Advantage

ARM's power advantage comes from power-saving techniques incorporated into the instruction set, which was clearly evident in the ARM9E-S processor introduced in May 1999. For example, by correctly identifying the adder among other functional blocks within the CPU as a power-hungry element, ARM incorporated bits in each instruction that would signify the need for the adder or another functional block. For all instruction not containing the bits, the adder or other functional blocks were powered down, thus reducing the core's power consumption.

Ironically, this technique achieved a power saving of only 15 percent over a CPU that executed the MIPS 1 instruction set. However, to gain this small power advantage, the ARM 9E architects made a number of design tradeoffs. For example, the ARM9E had 16 registers compared to the LX5180, which has 32 registers. Reducing registers can lower the apparent power consumption. But each time the CPU swaps data between memory and the register set, power savings is sometimes lost.

Another example can be found in the immediate instructions such as an op code containing data. The

ARM9E implemented the instructions with an associated immediate value of only 12 bits. Lexra's LX5180 immediate instructions have an associated value of 16 bits. Again, the ARM tradeoff can reduce power consumption slightly on a per-clock basis. However, the advantage is lost if the application calls for a larger immediate value. This is typically the case when an application's program size grows.

To its credit, the ARM core achieves linear power reduction with every process geometric shrink, but that's where power savings end. Until recently, ARM lacked a synthesizable core. It had to content itself with power reductions that came from each port of the ARM hard core to a specific IC fab. Furthermore, the ARM core typically runs at relatively high clock rates. The higher the clock frequency, the higher the power consumption.

Compelling ARM Alternative

The problem confronting SoC designers today is managing power in a more complex system that contains not only a RISC processor, but also a digital signal processor (DSP) as well as memory and large pin-count I/O. Lexra's 5180 RISC-DSP processor provides all the elements needed to address these concerns. The core's advantages include an architecture designed for the latest generation of process technology as well as a built-in, fully functional DSP that executes Lexra's Radiax extensions to the MIPS ISA.

The LX5180 offers inherent power savings. Lexra's processors reduced power consumption by using a custom register file that clocks data in only when the data changes. The LX5180 extends that practice across the entire processor through a simple design methodology change that allows clock-gated enable flip-flops.

Another way to save power comes from performing cache-read operations as needed and not during every cycle. For the LX5180 and LX5280, that enhancement offers up to 70 percent in data cache power

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dissipation. This benefit only reflects power dissipation in the cache operation and is additive to power savings in the processor itself.

A similar technique used in the LX5180 and LX5280 is to compute data as needed. For example, a shifter and an adder might operate on the same data, but if only the shifter results are needed, the adder is consuming power without producing results. Lexra processors eliminate such redundant operations unless they create critical-path issues.

ARM Vs Lexra Power Analysis

To show the low-power advantages of the new LX5180 processor, Lexra analyzed its power profile, the profiles of the LX5280 processor, and the ARM9E. The analysis used Powermill to obtain baseline data and extrapolations to derive design options and obtain results. The target foundry was TSMC, using the Artisan 0.18 micron, 1.8V standard cell library, which exhibits a power profile of 0.0450 micron W/MHz/gate.

The analysis (whose details are available from Lexra) found that application-related issues are critical when analyzing power consumption. Table 1 shows LX5180 and ARM9E power comparisons for three basic operations. The Lexra LX5180 has superior theoretical MAC throughput, which translates into improved DSP performance. The LX5180 and ARM 9E exhibited identical performance on Dhrystone MIPS (comparable RISC code performance), while the ARM 9E has a slight power advantage.

But the dot-product operation (a DSP-type function for multiplying two vectors) told a different story. In this case, the LX5180 performed the code example three times faster than the ARM9E. Assuming that the LX5180 was in sleep mode when not executing the application, the average power consumption plummeted. Another design alternative is to reduce the clock speed of the processor and system, which can provide similar gains, but could limit the flexibility of the system for a new application.

Application Level Comparison - DSP

	LX5180	ARM 9E
Max MAC Throughput @ 180 MHz	360 MMAC/s	180 MMAC/s
Dhrystone @ 180 MHz	190 MIPs	190 MIPs
Core Area	1.8 mm**2	1.5 mm**2
Power Consumption	0.8 mW/MHz	0.65 mW/MHz
Dot Product	1.5*N + 12	5*N
64 sample dot-product @ 180 MHz	600 ns	1800 ns
Average Power for dot-product	0.41	1

Table 1. *Comparison of core performance, area, power, and application-normalized power between the LX5180 and ARM 9E.*

Additional Comparisons on DSP Code

	LX5280	LX5180	ARM 9E
Vector Dot Product	0.5*N Cycles	1.5*N Cycles	5*N Cycles
Complex FFT N=256 Radiax-4	3200 Cycles	6200Cycles	12400 Cycle
Complex FFT N=1024 Radiax-4	14500 Cycles	29000Cycles	65000 Cycle
G.723.1 Full Duplex	13 MIPS	20 MIPS	72 MIPS

Table 2. *Comparison of application-specific performance of DSP algorithms on the LX5280, LX5180 and ARM 9E.*

Table 2 shows additional performance comparisons on DSP operations. The values for executing the G.723.1 code (standard Voice over Internet Protocol, or VoIP) are especially interesting because the ARM9E's performance was so poor that it was nearly impractical. A separate DSP unit would have been needed for VoIP applications, which would have further increased overall system power consumption.

Clearly, in applications that require DSP functions, the LX5180 offered significant power advantages over the ARM9E. Such applications include digital audio, PDAs, digital cameras, DSL modems, VoIP, and other broadband products. The LX5180's low cost, small die size, and low-power profile make it ideal for consumer applications. Moreover, because the LX5180's power consumption scales sublinearly with speed, the processor can push the performance envelope further on less power than competing processors. EJ

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