LEXRA	**Superscalar**	**LX4280**
	32-bit RISC Core	**Product Features**

- **Superscalar, Dual-Issue Architecture:** Executes two instructions simultaneously for sustained high performance. Pipeline A supports load/store addressing and coprocessor operations. Pipeline B executes multiply, divide, MAC operations, and instruction extensions. Both pipelines execute all ALU operations.
- **High Performance for Compute-Intensive Embedded Applications:** Operates at 200 MHz (worst-case) and delivers 260 Dhrystone MIPS. Entire processor subsystem (including MAC) occupies 5.2 mm^2 of silicon on a 0.18µm process and consumes 180 mW of power.
- **Low-Overhead Interrupts:** Eight new hardware-prioritized interrupts, each with dedicated interrupt vector, improve real-time interrupt response in telecom and datacom applications.
- **Object Code Compatible with LX4180:** All LX4180 code will run, unchanged but up to 35% faster, on the LX4280. Hardware MAC optional.
- **MIPS16™ Code Compression and EJTAG In-Circuit Emulation:** MIPS16 support provides up to 40% reduction in program size. Optional EJTAG interface supports full speed debug with real time instruction trace.
- **Development Tools:** Available from third party suppliers supporting the MIPS® architecture, including industry leaders Green Hills Software, Embedded Performance, and Wind River Systems. RTOS support includes NucleusPLUS, ThreadX™, and VxWorks™.
- **Easy to Integrate, Configure, and Extend:** Synchronous design with single phase clocking can be implemented with commercial EDA tools. Custom instructions and coprocessors can be added. Memory organization and size can be configured to support different applications.
- **Portable:** Available as a synthesizable RTL core or a SmoothCore™, an optimized hard macro ported to a specific foundry process.

LX4280 Architecture