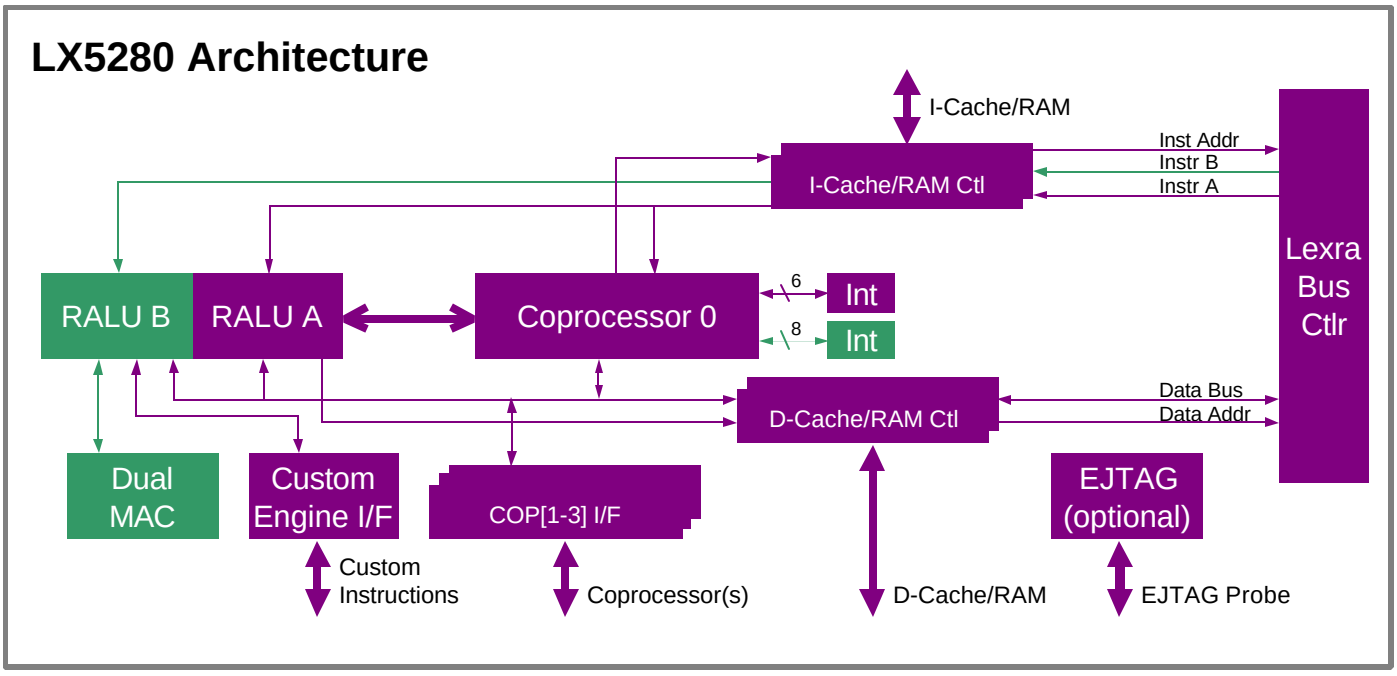
High Performance 32-bit RISC-DSP Core

LX5280 Product Features

- **First DSP Core Based on MIPS® ISA:** Superscalar, dual-issue pipeline with dual 16-bit/32-bit Multiply-Accumulate (MAC) engines integrated into the instruction flow. Executes MIPS® I instruction set* and Lexra RADIAX™ DSP extensions for true DSP arithmetic.
- **DSP Performance, Power and Efficiency:** Operates at 200 MHz (worst-case), delivering 400 million MAC operations per second. Entire RISC-DSP subsystem occupies less than 6 mm^2 of silicon on a 0.18µm process and consumes 225 mW of power.
- **RISC Architecture Ease-of-Use:** Leverages high-level language support by third party MIPS software tool suppliers for fast code development. Easy programming model for assembly coding of performance-critical inner loops.
- **RISC and DSP in a Single Processor Core:** Can eliminate the need for a separate DSP and microcontroller. Simplifies development., reduces chip size, cost and power consumption.
- **Development Tool Support:** Industry leaders including Green Hills Software and Embedded Performance offer software development tools for the LX5280 and RADIAX DSP extensions.
- **Easy to Integrate, Customize, and Extend:** Synchronous design with single phase clocking can be implemented with commercial EDA tools. Custom instructions and coprocessors can be added, and memory size and organization (cache architecture, cache vs. RAM) and other properties can be configured for a particular application.
- **MIPS16™ Code Compression and EJTAG In-Circuit Emulation:** MIPS16 support provides up to 40% reduction in program size. Optional EJTAG interface supports all required features of EJTAG 2.0.0 for full speed debug with real time instruction trace.
- **Portability:** Available as a synthesizable RTL core or SmoothCore™, an optimized hard macro that has been ported to a specific foundry process.

LX5280 Architecture



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