High Speed Packet Processing LX8000

32-bit RISC NPU Core Product Features

- **Up To Eight Hardware Contexts:** Allow software controlled zero delay switching to another thread of execution while the first thread waits for an external event such as a table look-up operation, maximizing packet processing throughput from minimal silicon area.
- **Dual-Port Data Memory:** Allows a high bandwidth device to source and sink DMA data at 64 bits per cycle.
- **Bit Field Manipulation Instructions:** Extend the MIPS ISA to enable efficient classification of IP packet headers.
- **Lexra Bus Extensions:** Increase the Lexra bus data width to 64 bits; facilitate the use of multiple contexts and multiple processors; provide for bus segmentation and bridging; allow transactions to release the bus while waiting for the return of target data.
- **Performance, Power, and Size:** Are unmatched in the industry. One core operating at 450 MHz consumes 0.425 watts in 4 mm^2 of silicon (with 4 contexts in a 0.15 µm process SmoothCore).
- **EJTAG Debug:** Extends the EJTAG 2.0.0 specification to the multi-processor and multi-context environment for on-chip debug. (optional)
- **Development Tools:** Available from third party suppliers supporting the MIPS architecture, including industry leaders Green Hills Software, Embedded Performance, and Wind River Systems.
- **Real-Time Operating System (RTOS) Support:** From industry leaders including NucleusPLUS™, ThreadX™, and VxWorks™.
- **Portability:** Available as a synthesizable RTL core or as a SmoothCore™, an optimized hard macro that has been ported to a specific foundry process. Foundry partners include IBM, TSMC, and UMC.