NVP

A Programmable OC-192c Powerplant

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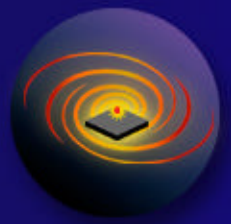
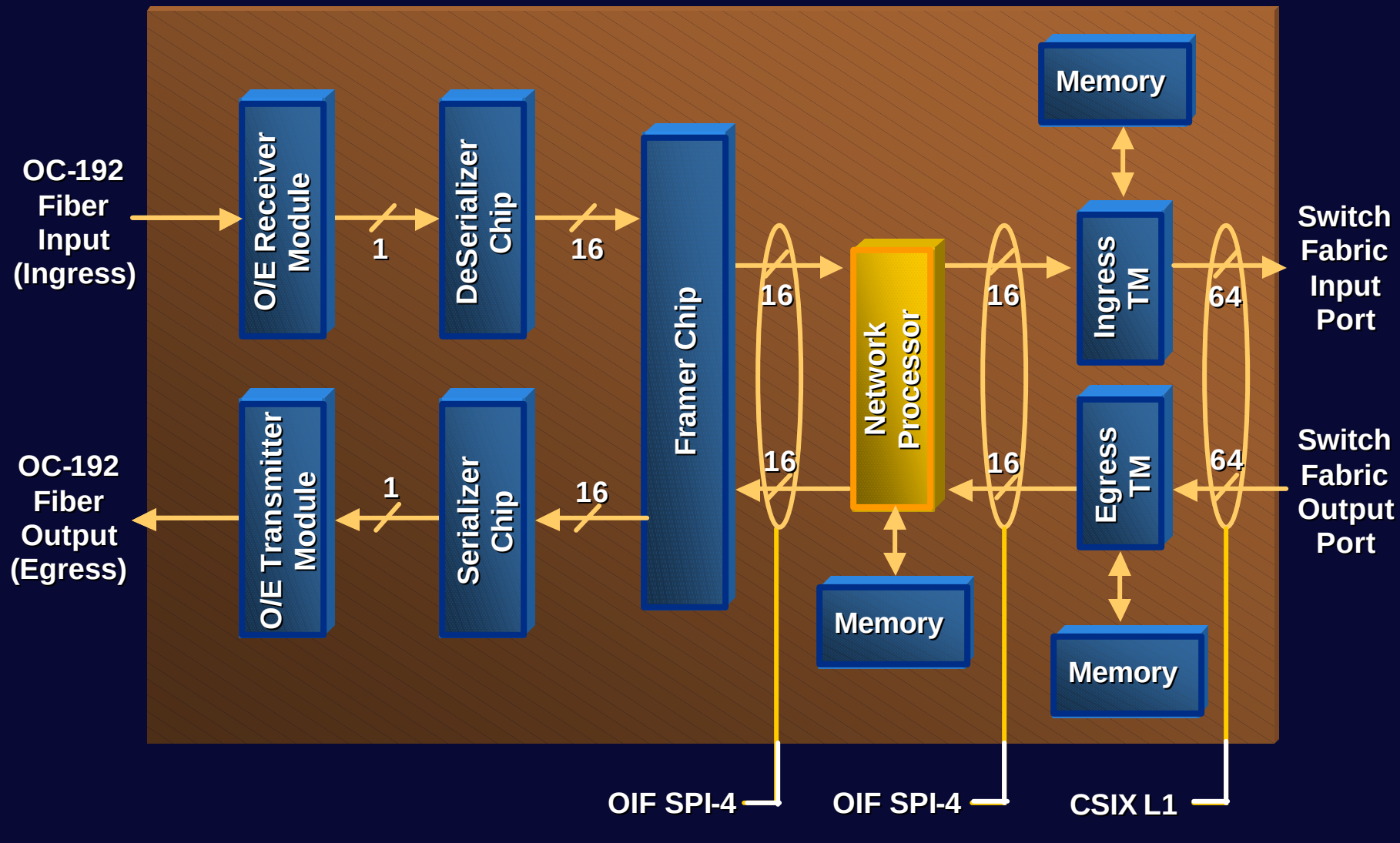


Outline

- Requirements for an OC-192c Router
- Architectural Alternatives
- NVP Architecture
- Results vs. Requirements
- Implementation
- Scaling to OC-768c
- Summary

Requirements for an OC-192c Router

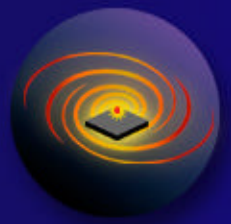
Block Diagram of Router Line Card



Requirements for an OC-192c Router

Summary of Network Processing Tasks

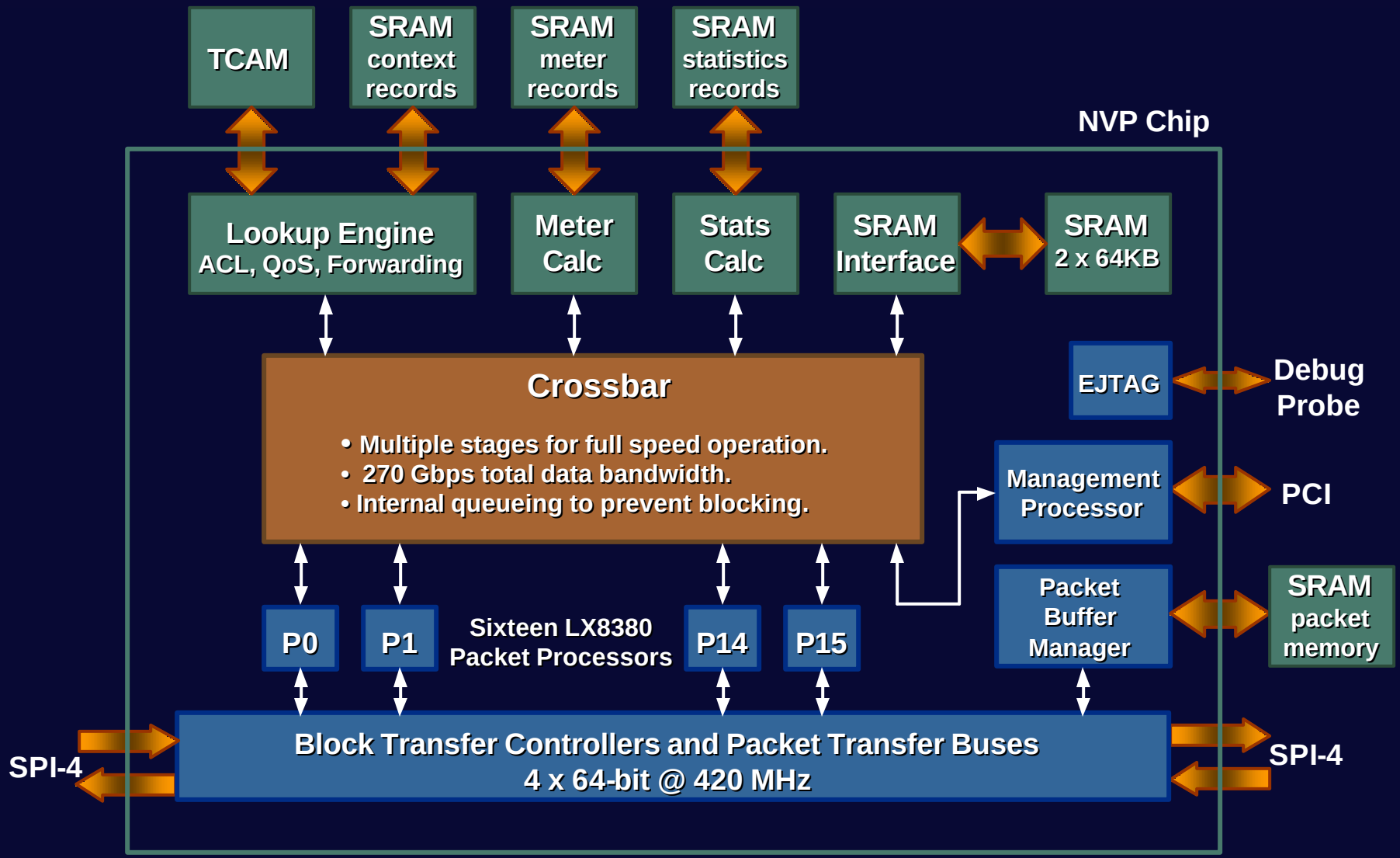
Ingress Packet Processing Tasks	RISC Cycles
1. Get next packet header to process	176
2. Parse header information	65
3. Access Control List (ACL) check	157
4. Quality of Service (QoS) determination	188
5. Forwarding lookup	192
6. Metering conformance check	184
7. Header modification	51
8. Format forwarding control header	23
9. Record statistics	282
10. Forward modified packet	27
Total Instructions/Packet	1,345
OC-192 Packets/Second (52-byte packets)	24 M
Required MIPS	32,280



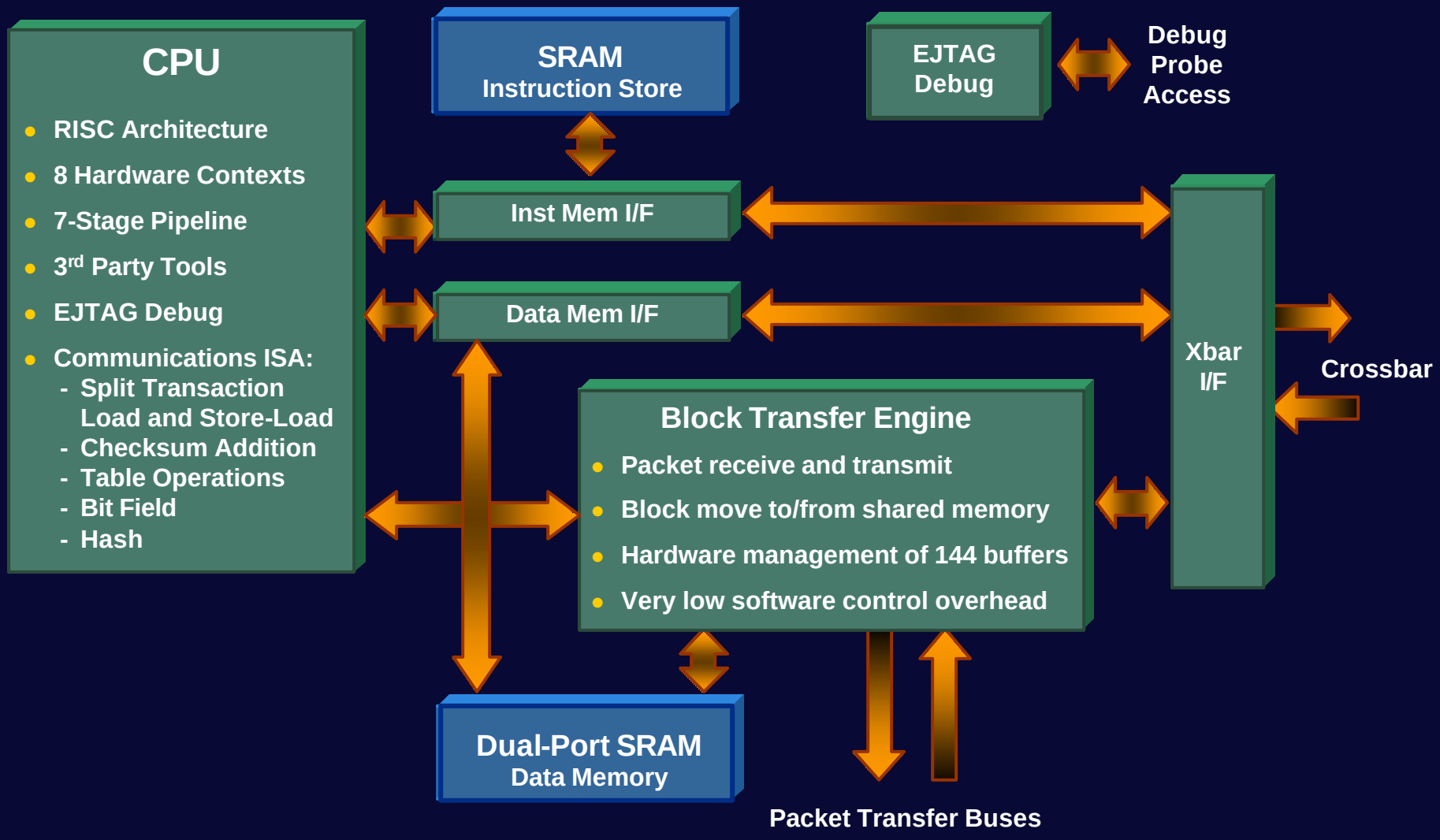
Architectural Alternatives

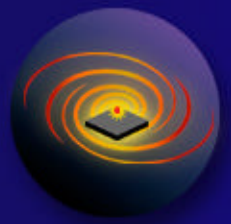
- High-end microprocessor → Requires 32 GHz!
- Network of task-specialized processors → Difficult to add new software
- Symmetric Multi-Processor (SMP) → NVP

NVP Architecture



LX8380 Processor Architecture



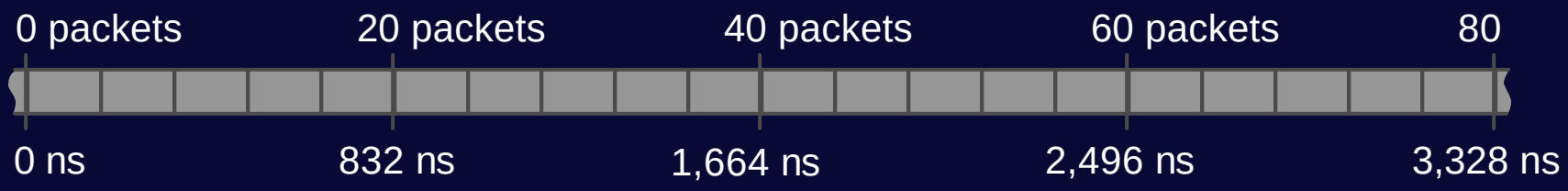


NVP Key Features and Benefits

- Complete general-purpose processing.
  Plus instruction set extensions for networking applications.
- Packet transfer to/from processor SRAM.
  Provides more flexibility than register-based transfer.
- Crossbar between processors and shared devices.
  Provides high data bandwidth for lookup, meter and statistics ops.
- Processors and devices support atomic operations.
  Sustains highly concurrent processing.
- Hardware scheduling of packet and crossbar transfers.
  Ensures high processor utilization and wire-speed operation.

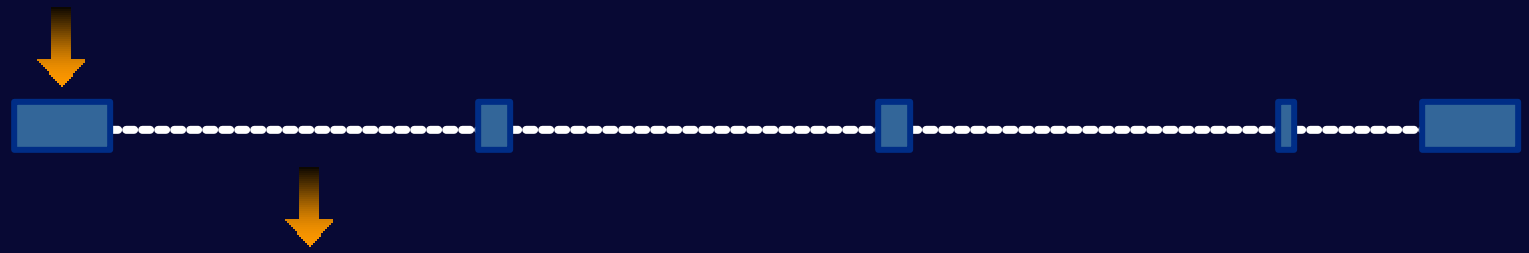
Per-Packet Compute Tasks

Packet Arrivals:



Processor Activity for One Packet:

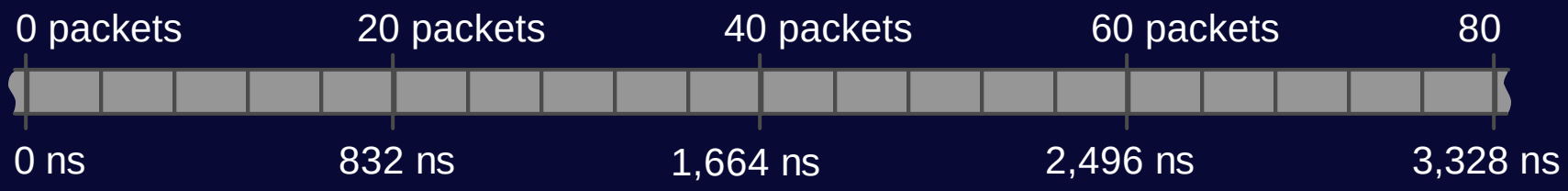
Parse header. Extract field for ACL lookup.



Wait for ACL result.

Per-Packet Compute Tasks

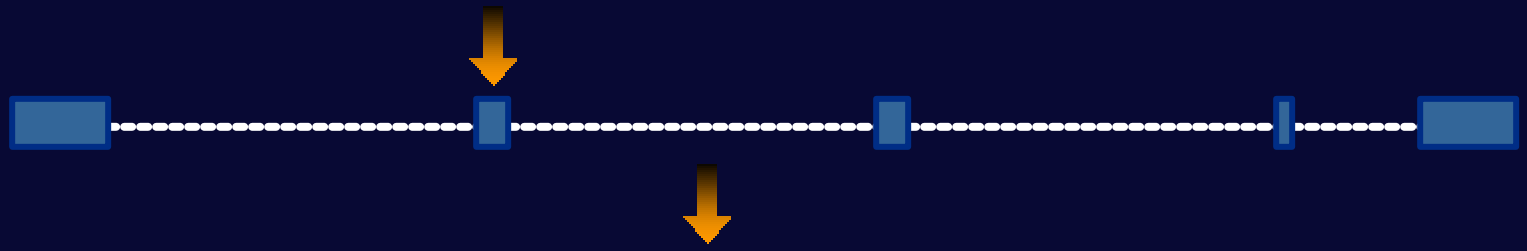
Packet Arrivals:



Processor Activity for One Packet:

Generate key for QoS lookup

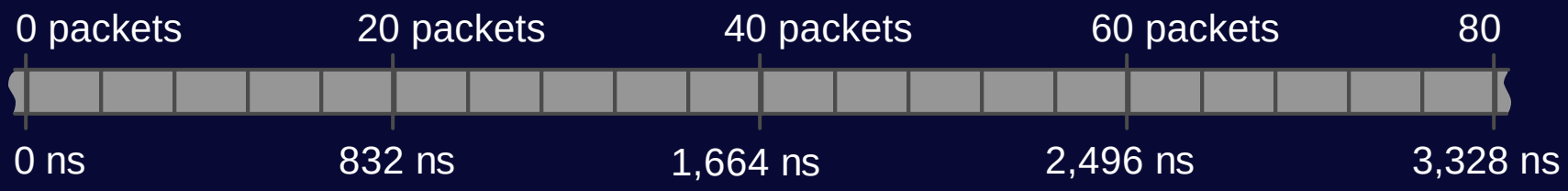
Multiple lookups improve TCAM hit rate and simplify TCAM maintenance.



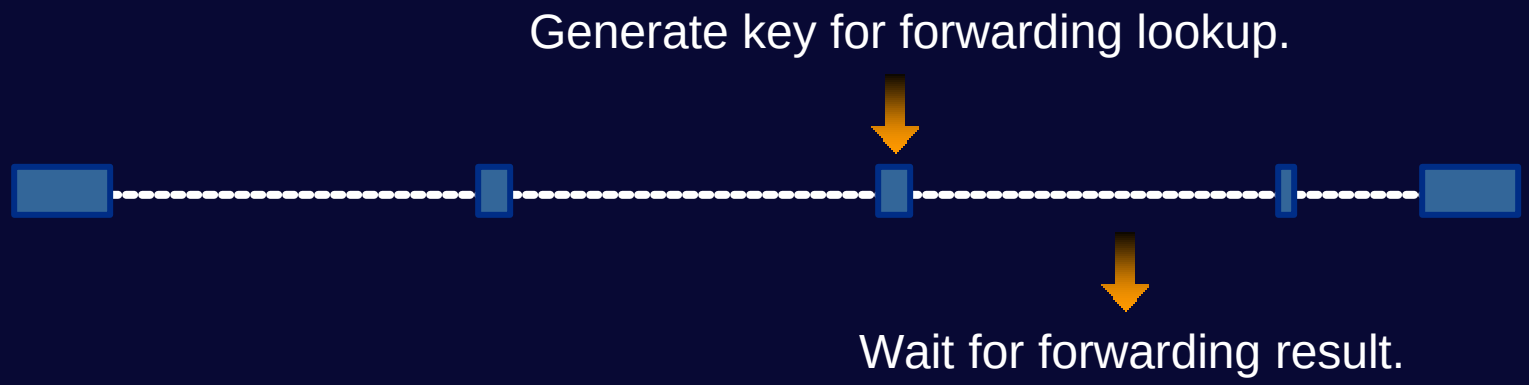
Wait for QoS result.

Per-Packet Compute Tasks

Packet Arrivals:

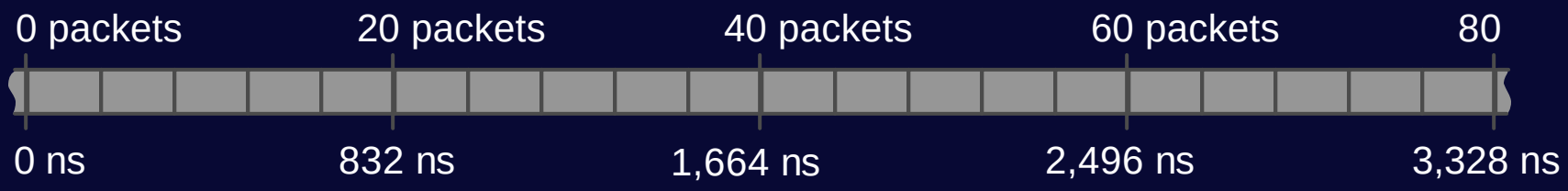


Processor Activity for One Packet:

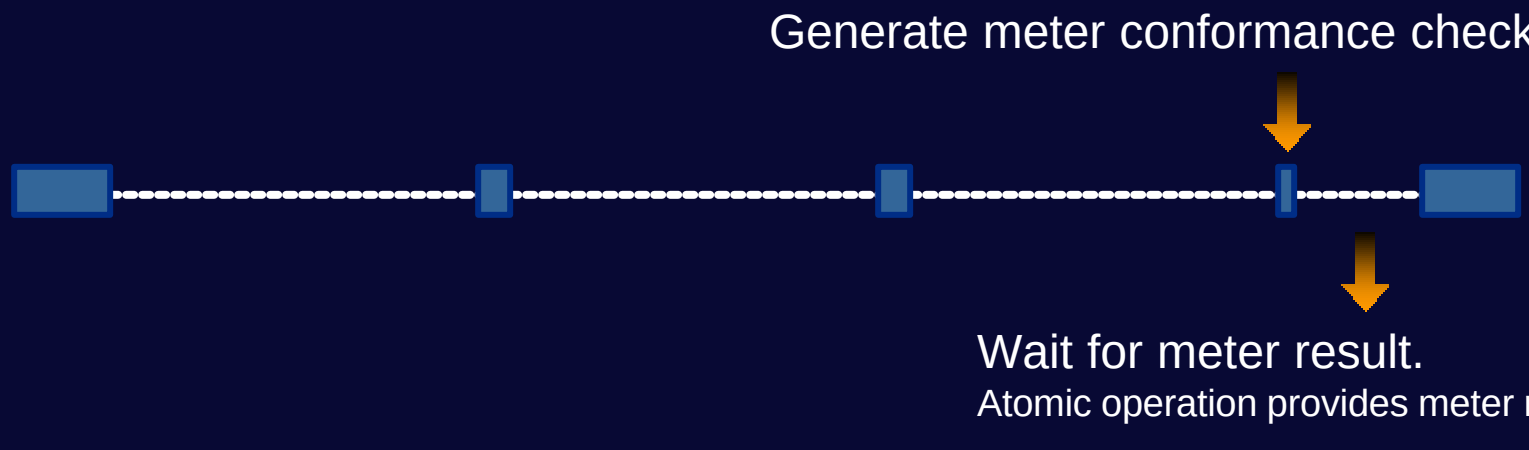


Per-Packet Compute Tasks

Packet Arrivals:

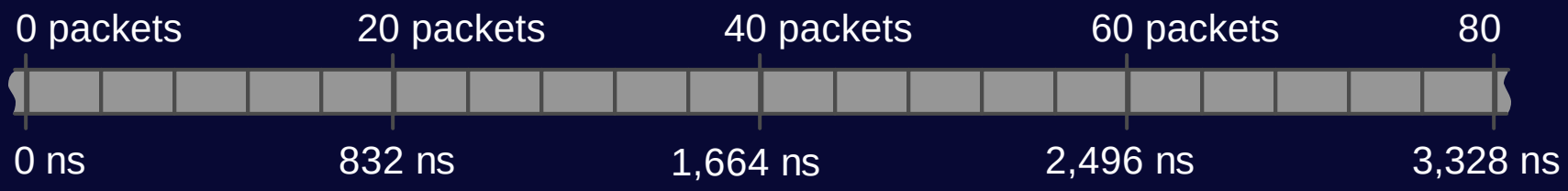


Processor Activity for One Packet:



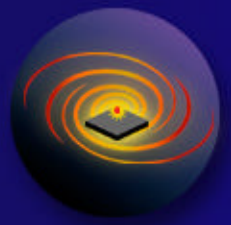
Per-Packet Compute Tasks

Packet Arrivals:



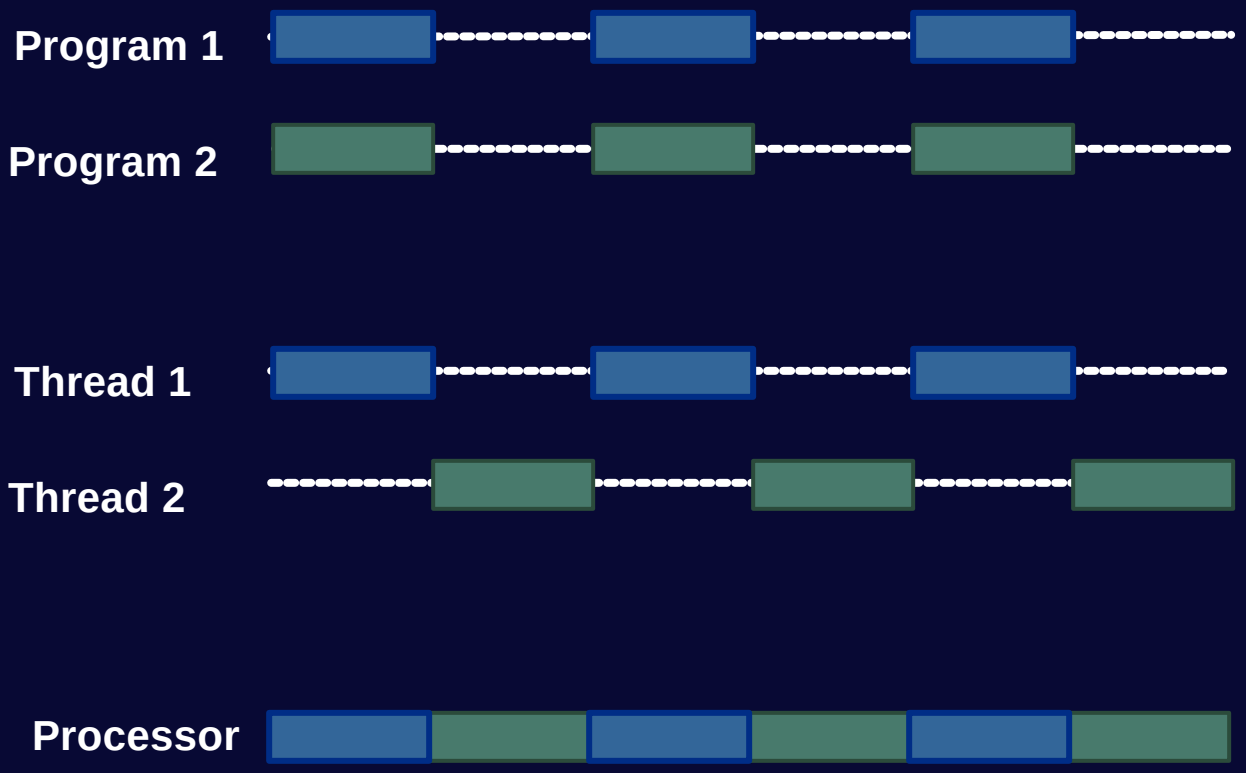
Processor Activity for One Packet:

Format header. Record statistics. Forward packet. Get new packet.



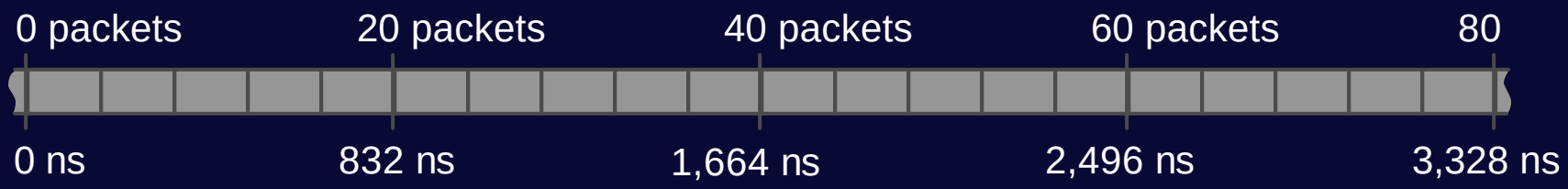
Multi-Threading

A Simplified Example

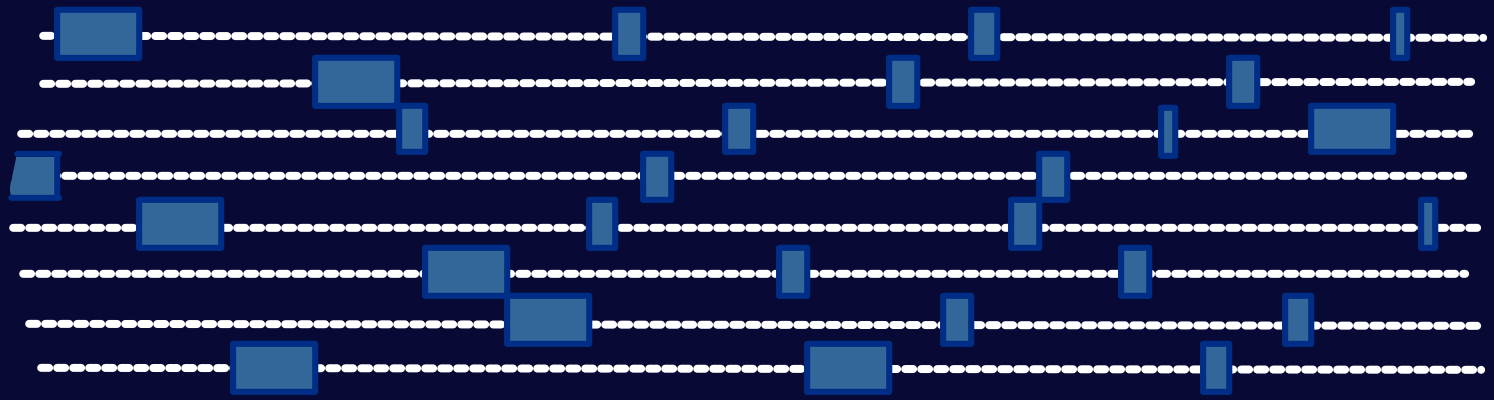


Real Multi-Threading

Snapshot from 16 Processor NVP Simulation



Activity of eight threads:



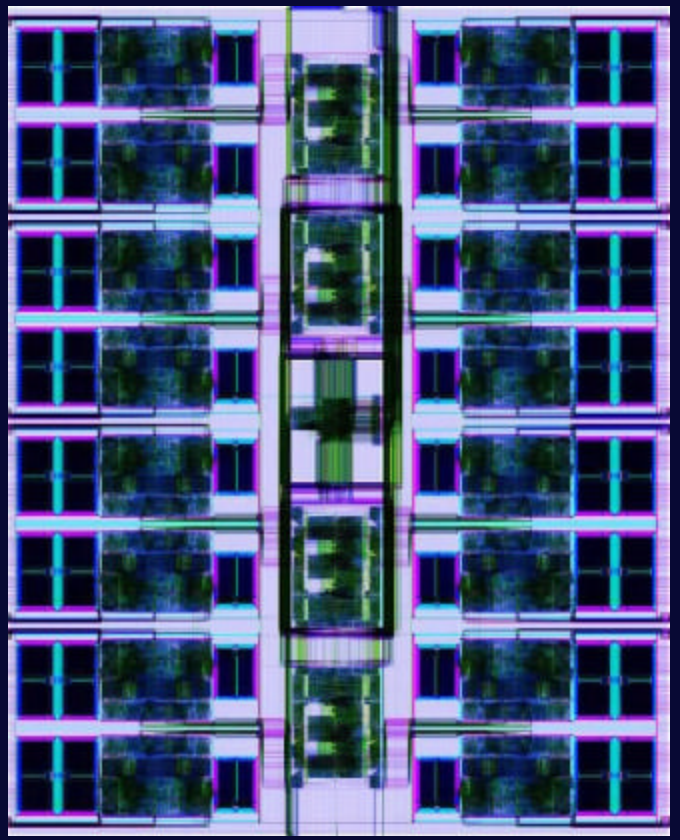
Activity of one processor:

Results vs. Requirements

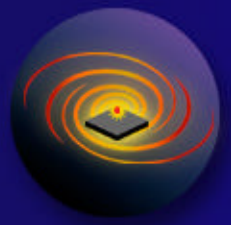
Ingress Packet Processing Tasks	RISC Cycles	NVP Cycles
1. Get next packet header to process	176	8
2. Parse header information	65	30
3. ACL check	157	19
4. QoS determination	188	10
5. Forwarding lookup	192	13
6. Metering conformance check	182	5
7. Header modification	51	24
8. Format forwarding control header	23	8
9. Record statistics	282	21
10. Forward modified packet	27	4
Total Instructions/Packet	1,345	142
OC-192 Packets/Second (52-byte packets)	24 M	24 M
Required MIPS	32,280	3,400

Implementation

- 420 MHz CPU clock, worst-case
- 6,720 MIPS
- 12 W power dissipation, worst-case
- 1157-pin BGA package
- 134 mm^2 die size
- Technology:
  - 0.13 um 6 level metal
  - Synthesized RTL model



Layout plot of 16 packet processors and crossbar



Scaling to OC-768c

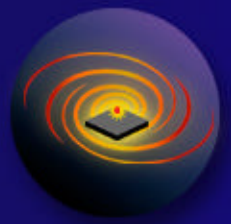
Attainable with 0.13 Micron Technology!

- 4X packet processing power:

  2.0X increase in processor count (from 16 to 32)
  1.4X increase in CPU clock (from 420 MHz to 600 MHz using structured custom)
  1.4X increase in ISA efficiency (more communications instructions)

  4X increase in packet processing power

- Other architectural issues:
  - Packet transfer requires
    SPI-5, LVDS pads, 128-bit buses, 256-bit wide DMEM
  - Shared IMEM to conserve area
    Permits extra 16 processors
  - Shared memory bandwidth
    Banked SDRAM
  - Enhanced hardware scheduling
    Improves processing latency and reduces packet buffer requirements



Summary

- *NVP is the first general-purpose multi-processor to deliver OC-192c performance*
- *NVP can be extended to become the first OC-768c network processor*